Remarks

Claims 1, 2, 6-11, 13-15, 18 and 19 are pending in the present application. In the Advisory Action dated May 17, 2005, the Examiner withdrew rejections under Inamori and Cho. However, all of claims 1, 2, 6-11, 13-15, 18 and 19 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Crampton. In view of the following remarks, reconsideration and withdrawal of these grounds of rejection is requested.

Claim Rejections Under 35 U.S.C. § 102

Claims 1, 2, 6-11, 13-15, 18 and 19 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Crampton (U.S. Pat. No. 5,767,721). For the reasons set forth below, reconsideration and withdrawal of this ground of rejection is respectfully requested.

The present invention comprises, in one exemplary embodiment, a switch 40 including a series switching transistor 42 and a shunt transistor 46 (See Fig. 3). A signal path 51 couples a radiofrequency (RF) input port 12 to an RF output port 14. A first control voltage V_{HI} is coupled to the signal path 51 near the input port 12. A second control voltage V is coupled to the series switching transistor 42 at its gate, and to the shunt transistor 46. The shunt transistor 46 is coupled to a feedforward capacitor 48 which assists in enhancing the isolation between input port 12 and output port 14, and improving the harmonic noise rejection of the switch 40.

As is well known to those of ordinary skill in the art, a "feedforward" capacitor, by definition, is coupled to at least two terminals of a transistor (e.g., gate and drain, gate and source).

With reference to Figure 3 of the present application, the feedforward capacitor 48 is coupled to the gate (G) and source (S) of the shunt transistor 46. This allows the source current (i_S) flowing from the source (S) and through the feedforward capacitor 48 to be fed back to the gate (through resistor 50), and thus effect the operation of the shunt transistor 46 by changing the gate-source voltage (V_{GS}) of the shunt transistor 46. This change in V_{GS} of the shunt transistor 46 allows the transistor to handle larger drain-source currents (i.e., i_{DS}) without substantially affecting operation.

The "feedforward" arrangement shown in Figure 3 of the present application allows for the gate-source voltage (V_{GS}) of the shunt transistor 46 to increase at the same time the drain-source current (i_{DS}) is increased, by feeding the drain-source current (i_{DS}) back to the gate of the shunt transistor through the "feedforward" capacitor 48 and the resistor 50. In particular, the increasing current flowing through "feedforward" capacitor 48 and the resistor 50 creates an increasing voltage across the resistor, which in turn, increases the gate-source voltage (V_{GS}) of the shunt transistor 46.

In operation, when the second control voltage V is above the pinchoff voltage (V_p) of the series switching transistor 42 (e.g., V_{p42}), the series switching transistor 42 is turned ON and the shunt transistor is turned OFF. Alternatively, when the second control voltage V is below the pinchoff voltage of the series switching transistor (V_{p42}) and the first control voltage V_{HI} is greater than V_{p42}, the series switching transistor 42 is turned OFF and the shunt transistor is turned ON. For example, if V_{p42} were 2 Volts, any second control voltage V above 2 Volts would bias series switching transistor 42 ON and bias shunt transistor OFF. Similarly, if the

second control voltage V dropped to zero (0) Volts, and V_{HI} were maintained above V_{p42} at all times (e.g., at say 5 Volts), the series switching transistor 42 would be biased OFF and shunt transistor 46 would be biased ON. Thus, both the series switching transistor 42 and the shunt transistor 46 may be controlled by a single control signal (e.g., the second control signal V), an action which could not have been accomplished by the prior art circuit shown in Figure 1 (which includes two control voltages V and V') (emphasis added).

Independent claim 1 now recites:

> An integrated circuit switch comprising: at least two signal ports coupled by a signal path, the signal path including a channel of at least one series FET; a shunt path coupled to ground and including a channel of a shunt FET; a first control voltage applied to the signal path; and, a second control voltage applied to a gate of the series FET and to a drain/source of the shunt FET, wherein the shunt path includes at least one feedforward capacitor, said feedforward capacitor being coupled to a source terminal and a gate terminal of the shunt FET. [emphasis added].

Thus, claim 1 requires a circuit including a "first control voltage" applied to a signal path which includes a "series FET," and a "second control voltage" applied to the gate of the series FET and the source or drain of a "shunt FET." Claim 1 also requires at least one "feedforward capacitor" coupled to the shunt FET at both its source and gate terminals. Crampton fails to disclose, teach or suggest such an invention.

Crampton teaches a switch circuit 56 with an RF input 58 and an RF output 70. The switch circuit 56 also includes depletion mode FETs 64, 80 which are coupled to a control voltage V1. Crampton does not disclose, teach or suggest a "first control voltage" applied to the signal line connecting the RF input 58 to the RF output 70. Additionally, Crampton does not

disclose, teach or suggest a "feedforward capacitor" coupled to FET 80. In fact, the only capacitors coupled to FET 80 are isolation/coupling capacitors 74, 84.

The capacitors 74, 84 are not "feedforward" capacitors. The term "feedforward" has an accepted definition in the art, and the capacitors 74, 84 clearly do not meet with that definition as they are only coupled to one terminal of the respective transistors 64, 80 (i.e., drain (D) or source (S)), and do not affect the gate-source voltage (V_{GS}) of the FET 80. In fact, there is no way the capacitors 74, 84 could affect the gate-source voltage (V_{GS}) of the FET 80, as neither one is coupled to the gate (G) of the FET (i.e., capacitor 74 is coupled to drain/source terminal of FET 80, and capacitor 84 is coupled between the drain/source terminal of the FET 80 and ground). The capacitors 74, 84 shown in Crampton clearly provide isolation, and not any type of feedforward function.

Additionally, the feedforward capacitor is required to be connected to "a source terminal and a gate terminal of [a] shunt FET." The capacitors 74, 84 shown in Crampton are not coupled to the gate of the associated FET 80. Therefore, Crampton cannot meet the limitation of claim 1 of a "feedforward capacitor" coupled to "a source terminal and a gate terminal of the shunt FET."

Accordingly, Crampton fails to disclose, teach or suggest a switch circuit including a "first control voltage" applied to a signal path which includes a "series FET," and a "second control voltage" applied to the gate of the series FET and the source or drain of a "shunt FET," where the shunt FET is gate and source coupled to a "feedforward capacitor," reconsideration and withdrawal of this ground of rejection with respect to independent claim 1, is respectfully requested.

Independent claims 2, 6, 8 and 9 have been amended to include similar limitations to those discussed above with reference to claim 1. Therefore, for at least those reasons discussed above with respect to claim 1, reconsideration and withdrawal of this rejection with respect to claims 2, 6-11, 13-15, 18 and 19 is also respectfully requested.

Conclusion

In view of the foregoing remarks, Applicants submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

Respectfully submitted,

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